REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3, 5, 14, and 15 are presently active. Claim 16 has been cancelled without prejudice; and Claim 1 has been amended by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 1-3, 5, and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,642,160 to <u>Burgess</u> (hereinafter "the '160 patent") in view of U.S. Patent No. 5,747,358 to <u>Gorrell et al.</u> (hereinafter "the '358 patent").

Amended Claim 1 is directed to a printed wiring board, comprising: (1) an insulating layer having a first surface and a second surface; (2) a plurality of circuit patterns formed by etching metal foils laminated on at least the first surface and the second surface of the insulating layer, wherein a circuit pattern on the first surface of the plurality of circuit patterns is a line through which an electric current flows; (3) a via formed on said insulating layer; (4) a first plating layer having a first portion that covers an inner surface of the via, a second portion that covers a circuit pattern that is on the first surface and which continues to one end of the via, and a third portion that covers a part of the circuit pattern formed on the first surface at a location outside the via; and (5) a second plating layer laminated on the first plating layer and electrically connecting the circuit pattern formed on the first surface with the circuit pattern that closes the other end of the via. Moreover, the second plating layer and the third portion of the first plating form a thick portion having an increased thickness on a part of the circuit pattern formed on the first surface, and a current capacity of the circuit pattern is increased at the thick portion. Claim 1 has been amended to clarify that (1) the first plating layer includes a third portion that covers part of the circuit pattern formed on the

first surface at a location outside the via, (2) the second plating layer and the third portion of the first plating layer form a thick portion having an increased thickness on a part of the circuit formed on the first surface, and (3) the current capacity of the circuit pattern is increased at the thick portion. The changes to Claim 1 are supported by the originally filed specification and do not add new matter.²

Applicants respectfully submit that the rejection of Claim 1 is rendered moot by the amendment to Claim 1 herein.

Regarding the rejection of Claim 1 under 35 U.S.C. § 103, the Office Action asserts that the '160 patent discloses everything in Claim 1 with the exception of the second plating layer, and relies on the '358 patent to remedy that deficiency.

The '160 patent is directed to a circuit board including an insulating layer having a first surface and a second surface, a plurality of wiring layers laminated on the first and second surfaces, and a via formed on the insulating layer. Note that layer 38 of the '160 patent is stacked to cover all of the wiring layers formed on the first and second surfaces of the insulating layer. Accordingly, the '160 wiring layers on the first and second surfaces are of uniform thicknesses. However, as admitted in the Office Action, the '160 patent fails to disclose a second plating layer laminated on the first plating layer and electrically connecting a circuit pattern on the first surface with a circuit pattern that closes the other end of the via. Moreover, Applicants submit that the '160 patent fails to disclose a third portion that covers a part of the circuit pattern formed on the first surface at a location outside the via, as recited in amended Claim 1. Further, the '160 patent fails to disclose that the second plating layer and the third portion of the first plating layer form a thick portion having an increased thickness on a part of the circuit formed on the first surface, and that the current capacity of the circuit pattern is increased at the thick portion, as recited in amended Claim 1.

² See Figure 31 and page 42, lines 17-24, and page 44, lines 18-26, of the specification.

Turning now to the secondary reference, the '358 patent is directed to a method of forming raised metallic contacts on electrical circuits. In particular, the metal layer disclosed in Figure 16 of the '358 patent establishes an electrical connection between (1) the pads, and (2) the circuit board and the conductive layer that forms the bump 50. Note that the metallic layer disclosed in the '358 patent is formed only inside a via and in the vicinity of the opening end of the via. Moreover, the pattern disclosed in Figure 16 has a uniform thickness except in the area of the via. However, the '358 patent fails to disclose that the second plating layer and the third portion of the first plating layer form a thick portion having an increased thickness on a part of the circuit formed on the first surface, and that the current capacity of the circuit pattern is increased at the thick portion, as recited in amended Claim 1.

Thus, no matter how the teachings of the '160 and '358 patents are combined, the combination does not teach or suggest a second plating layer laminated on a first plating layer wherein the second plating layer and a third portion of the first plating layer form a thick portion having an increased thickness on a part of the circuit pattern formed on the first surface, or that the current capacity of the circuit pattern is increased at the thick portion, as recited in amended Claim 1.

Thus, it is respectfully submitted that independent Claim 1 (and dependent Claims 2, 3, 5, 14, and 15) patentably define over the '160 and '358 patents.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C.

Gregory J. Maier

Attorney of Record

Registration No. 25,599

furnish Souhas

Surinder Sachar

Registration No. 34,423

22850

(703) 413-3000

Fax #: (703) 413-2220

GJM/SNS/KMB/sy/law/kst

I:\atty\kmb\210854us-am.doc

Docket No.: 210854US2S

Marked-Up Copy

Serial No: 09/899,156

Amendment Filed on: 4-7-3

IN THE CLAIMS

1. (Three Times Amended) A printed wiring board, comprising:

an insulating layer having a first surface, and a second surface located on an opposite side of said first surface;

a plurality of circuit patterns formed by etching metal foils laminated on at least said first surface and said second surface of said insulating layer, wherein a circuit pattern on the first surface of said plurality of circuit patterns is a line through which an electric current flows;

a via formed on said insulating layer, said via having one end opened on said first surface of said insulating layer and the other end closed by a circuit pattern of said plurality of circuit patterns formed on a part of said insulating layer other than said first surface;

a first plating layer having (1) a first portion that covers an inner surface of said via and a circuit pattern of said plurality of said circuit patterns that closes said other end of said via and which is exposed within said via, [and] (2) a second portion that covers a circuit pattern of said plurality of said circuit patterns that is on said first surface and which continues to said one end of said via[;], and (3) a third portion that covers a part of said circuit pattern of said plurality of circuit patterns formed on the first surface at a location outside the via, wherein the first to third portions are simultaneously processed; and

a second plating layer laminated on said first plating layer and electrically connecting [a] said circuit pattern of said plurality of circuit patterns formed on said first surface with said circuit pattern of the plurality of circuit patterns that closes said other end of said via[.], wherein the second plating layer and the third portion of the first plating layer form a thick portion having an increased thickness on a part of said circuit pattern formed on the first surface, and a current capacity of the circuit pattern is increased at the thick portion.

16. (Cancelled)